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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09 970,593	10 04 2001	Akira Yoshizawa	09792909-5237	1195

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EXAMINER
TRAN, TAN N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05 21 2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)
09/970 593	YOSHIZAWA ET AL
Examiner	**Art Unit**
TAN N TRAN	2826

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2001*

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4)☐ Interview Summary (PTO-413) Paper No(s). _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-8 in Paper No. 9 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Drawings

2. Figure 11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

3. If applicant is aware of any relevant prior art, he/she requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. **609.**

Claim Objections

4. Claims 2-8 are objected to because of the following informalities:

In claims 2-8, line 1, "A semiconductor" should be changed to - The semiconductor --.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muramatsu et al. (6,420,664) in view of Otsuka (5,949,142).

With regard to claim 1, Muramatsu et al. discloses a semiconductor chip having a plurality of electrodes 12 formed on the surface of thereof; an interposer substrate 40 on which the semiconductor chip 10 is mounted; a core substrate 18 constituting the base of the interposer substrate 40; built-up layers built on only one surface on the core substrate 18; the electrodes 12 on the core substrate 18 and chip 12. (Note figs. 1,17,18,19C of Muramatsu et al.)

Muramatsu et al. does not disclose an anisotropic conductive layer which is formed on the other surface of the core substrate, and via which the semiconductor chip is mounted on the core substrate; and the electrodes on the core substrate and those on the semiconductor chip.

However, Otsuka discloses an anisotropic conductive layer 6 which is formed on the other surface of the substrate 5, and via which the semiconductor chip 2 is mounted on the substrate 5; and the electrodes 2a on the substrate 5 and those on the semiconductor chip 2.

Therefore, it would have been obvious to one of ordinary skill in the art to form the Muramatsu et al.'s device an anisotropic conductive layer which is formed on the other surface of the core substrate, and via which the semiconductor chip is mounted on the core substrate;

and the electrodes on the core substrate and those on the semiconductor chip such as taught by Otsuka in order to prevent the chip surface from being damaged.

With regard to claim 2. Muramatsu et al. and Otsuka disclose all the claimed subject matter except for each of the built-up layers built on the core substrate has an elastic modulus of 5000 Mpa or below. However, it would have been obvious to one of ordinary skill in the art to form each of the built-up layers built on the core substrate has an elastic modulus of 5000 Mpa or below in order to reduce the stress that may damage the vias.

With regard to claim 3. Muramatsu et al. and Otsuka disclose all the claimed subject matter except for the core substrate is formed of a material having an elastic modulus closer to that of the semiconductor chip than to that of the built-up layer. However, it would have been obvious to one of ordinary skill in the art to form the core substrate having an elastic modulus closer to that of the semiconductor chip than to that of the built-up layer in order to reduce the stress that may damage the vias.

With regard to claim 4. Muramatsu et al. discloses each of the built-up layers has curved wiring 26 formed on the surface thereof so as to relax stress. (Note fig. 18 of Muramatsu et al.).

With regard to claim 5. Muramatsu et al. and Otsuka disclose all the claimed subject matter except for the core substrate is formed of a material having a thermal expansion coefficient closer to that of the semiconductor chip than that of the built-up layers, and wherein the core has a thickness of 0.5 mm or below. However, it would have been obvious to one of ordinary skill in the art to form the core substrate is formed of a material having a thermal expansion coefficient closer to that of the semiconductor chip than that of the built-up layers.

and wherein the core has a thickness of 0.5 mm or below in order to conduct mounting very reliably.

Allowable Subject Matter

6. Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-8 are allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as reinforced patterns are formed at the positions corresponding to the electrodes on the semiconductor chip as recited in claim 6.

Conclusion

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

April 2003